Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **INPUT-**
2. **INPUT+**
3. **V-**
4. **OUTPUT**
5. **V+**

**.052”**

**.047”**

**2 1**

**5**

**4**

**3**

**L**

**M**

**1**

**0**

**7**

**C**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035 x .0035”**

**Backside Potential:**

**Mask Ref: LM107C**

**APPROVED BY: DK DIE SIZE .047” X .052” DATE: 6/28/18**

**MFG: NATIONAL THICKNESS .009” P/N: LM107**

**DG 10.1.2**

#### Rev B, 7/19/02